REMARKS/ARGUMENTS

Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Adachi (JP401319094). Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of applicant's admitted prior art. Claim 12 is rejected under 35 U.S.C. 103(a) as being anticipated by Adachi.

1. Rejection of claims 1-2 and 4:

Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Adachi (JP401319094).

Regarding to claim 1, Adachi discloses a driving circuit of a liquid crystal display device comprising: a substrate (101, Fig. 7); at least two driver integrated circuit (IC) chips (101, 109, Fig. 1) positioned on the substrate; and an impedance device (206, 207, 208, Fig. 3) electrically connected between the two driver IC chips. The impedance device inherently reduces a difference between respective input voltages being input into the two driver IC chips.

Regarding to claim 2, Adachi discloses the substrate comprises a plurality of scanning lines (122, Fig. 8) and a plurality of signal lines thereon (119, Figs. 1 and 8).

Regarding to claim 4, Adachi discloses the driver IC chips are used for outputting image signals to the signal lines (see Figs. 1 and 8).

Response:

In the present application, an impedance device is utilized to connect the driver IC chips in place of the traditional transmitting lines. In comparison with the traditional

transmitting lines, the impedance device can reduce the equivalent impedance (Z) of the responding current of a controlling signal, so that the voltage drop on the impedance device can be reduced. Therefore, a difference between respective input voltages being input into the driver IC chips can be effectively decreased, and the driver IC chips can obtain approximately equal input voltages.

The Examiner considers that Adachi discloses the similar device structure to the present application with an impedance device 206, 207, 208. However, according to page 3 of Adachi's specification, **the resistors 205, 206, 207, 208 are equivalent resistors of the clock wiring section 114, and the capacitor 209 is a parasite capacitor between the electrode section 201 and the clock wiring section 114.** In Adachi's disclosure, the resistance of the transmitting line of the clock wiring section 114 (such as the resistors 206, 207, 208), and the parasitic capacitance of these transmitting lines (such as the capacitor 209) are not tangible devices, and result in the unwanted delay of the timing signal.

The impedance device in the present application is a tangible device, shown in Fig. 4A, Fig. 5, Fig. 6A, Fig. 6B, to reduce a difference between respective input voltages being input into the two driver IC chips. In contrast, the resistors 206, 207, 208 are merely for showing the equivalent resistances of the clock wiring section 114. The resistors 206, 207, 208 represent the clock wiring section 114, and **the resistors 206, 207, 208 are corresponding to the traditional transmitting lines, not the impedance device of the present application**. Adachi's disclosure never teaches or mentions to reduce a difference between respective input voltages being input into the driver IC chip 108 and the driver IC chip 109. As a result, applicant believes that *Adachi does not teach a tangible impedance device for reducing a difference between respective input voltages being input into the two driver IC chips*. Since the concrete structure of Adachi's disclosure is different from the concrete structure of the present application, and Adachi's

specification does not disclose all the limitations in our claim 1, claim 1 should be patentable in comparison with Adachi's disclosure. Reconsideration of claim 1 is respectfully requested.

As claims 2 and 4 are dependent upon claim 1, they should be allowable if claim 1 is allowable. Reconsideration of claims 2 and 4 is respectfully requested.

2. Rejection of claims 3 and 13:

Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of applicant's admitted prior art.

Regarding to claim 3, Adachi does not explicitly disclose connecting driver circuits (driver IC chips) to the scanning lines.

The admitted prior art discloses connecting a plurality of driver IC chips (22, Fig. 1) to a plurality of scanning lines.

In light of the admitted prior art, it would have been obvious to one of ordinary skill in the art to connect the IC chips to Adachi's scanning lines because there must be driver circuits for driving the scanning lines.

Regarding to claim 13, Adachi does not explicitly disclose the liquid crystal display device is designed by applying wiring on array (WOA) technology.

The admitted prior art discloses a liquid crystal display device is designed by applying wiring on array (WOA) technology to reduce a production cost [0008].

In light of the admitted prior art, it would have been obvious to one of ordinary skill

in the art to connect the wiring on array (WOA) technology on Adachi's liquid crystal display device to reduce a production cost.

Response:

Adachi's disclosure is applied for operating a display device with high-speed clocks by delaying the clocks in corresponding to the delay of a start pulse between signal driving ICs. Accordingly, Adachi does not disclose the driver IC chips 108, 109 are used for outputting switching or addressing signals to the scanning lines. Adachi's disclosure never teaches or mentions to utilize an impedance device for reducing a difference between respective input voltages being input into the driver IC chip 108 and the driver IC chip 109. The present application utilizes an impedance device to connect the driver IC chips in place of the traditional transmitting lines. Since Adachi does not teach the impedance device as mentioned above, the combination of the applicant's admitted prior art and Adachi's scanning lines cannot disclose all the limitations in claim 1 of the present application.

Besides, since Adachi does not disclose the liquid crystal display device using WOA technology nor teach an impedance device electrically connected between the two driver IC chips, it is unobvious to one of ordinary skill in the art to form the impedance device designed by applying WOA technology in the present application.

As claims 3 and 13 are dependent upon claim 1, they should be allowable if claim 1 is allowable. Reconsideration of claims 3 and 13 is respectfully requested.

3. Rejection of claim 12:

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi.

Adachi further discloses a conductive layer is positioned between each of the driver

IC chips and the impedance device (see connections in Fig. 3), each of the driver IC chips being capable of receiving an approximately identical input voltage through each of the transparent conductive layers. Adachi does not disclose the conductive layer is transparent. However, it is considered a matter of obvious design choice to make Adachi's conductive layer transparent because this does not provide any unexpected result.

Response:

The present application utilizes an impedance device to connect the driver IC chips in place of the traditional transmitting lines. Since Adachi does not teach an impedance device to reduce a difference between respective input voltages being input into the driver IC chips, it is unobvious to one of ordinary skill in the art to form the present application according to Adachi's disclosure, and claim 1 should be patentable in consideration of 35 U.S.C. 103(a). As claim 12 is dependent upon claim 1, it should be allowable if claim 1 is allowable. Reconsideration of claim 12 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu

Date: September 19, 2006

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